PRODUCT SPECIFICATION

F89FTSM13

Wi-Fi Single-band 1T1R Module Datasheet

Version:v1.9

Customer: _____

Customer P/N:_____

Signature:_____

Date:_____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186 Website:www.fn-link.com

F89FTSM13 Module Datasheet

	Part NO.	Description
Ordering Information	FG89FTSM13-W4	RTL8189FTV-VQ1,802.11b/g/n ,1T1R,12.0*12.0 ,SDIO2.0, no shielding,PCB V04

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2018/08/06	New version	lzm	lzm	-
V1.1	2018/08/07	Modified RF Spec	lzm	lzm	-
V1.2	2020/09/29	Modified Operating Temperature Spec	FC	FC	-
V1.3	2020/12/14	Update PCB thickness dimension	LXY	LXY	-
V1.4	2022/2/10	Update the specification format Update Reference Design	FC	LXY	QJP
V1.5	2023/09/18	Add the module bottom welding pad Update Package information Update Recommended Reflow Profile	LXP	LXY	QJP
V1.6	2023/10/26	Update Host Interface Timing Diagram	LXP	LXY	QJP
V1.7	2023/12/01	Add Certificate No Add TVS Manufacturer	Lxp	LXY	Qjp
V1.8	2024/10/11	Update Marking Description	Lxp	LXY	QJP
V1.9	2025/02/12	Update UART and GPIO interafce Delete Marking Description	LXP	LXY	QJP

1. General Description

1.1 Introduction

F89FTSM13-W4 is a highly integrated and excellent performance Wireless LAN (WLAN) SDIO network interface device. High-speed wireless connection up to 72.2 Mbps.

The general hardware for the module is shown in Figure 1. This WLAN Module design is based on Realtek RTL8189FTV. It is a highly integrated single-chip 1*1 SISO WLAN SDIO network interface controller complying with the 802.11n specification. It combines a MAC, a 1T1R capable baseband, and RF in a single chip. It is designed to provide excellent performance with low power Consumption and enhance the advantages of robust system and cost-effective.

1.2 Description

Model Name	F89FTSM13
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 12 x 12 x1.6 mm
Wi-Fi Interface	Support SDIO2.0 / GPIO
OS supported	Android /Linux
Operating temperature	-10°C to 70°C
Storage temperature	-40°C to 80°C

1.Chipset recommanded low temperature at 0°C,Module actually test passed at -10°

2. Features

General

- Enterprise level security which can apply WPA/WPA2 certification for WiFi

PHY Features

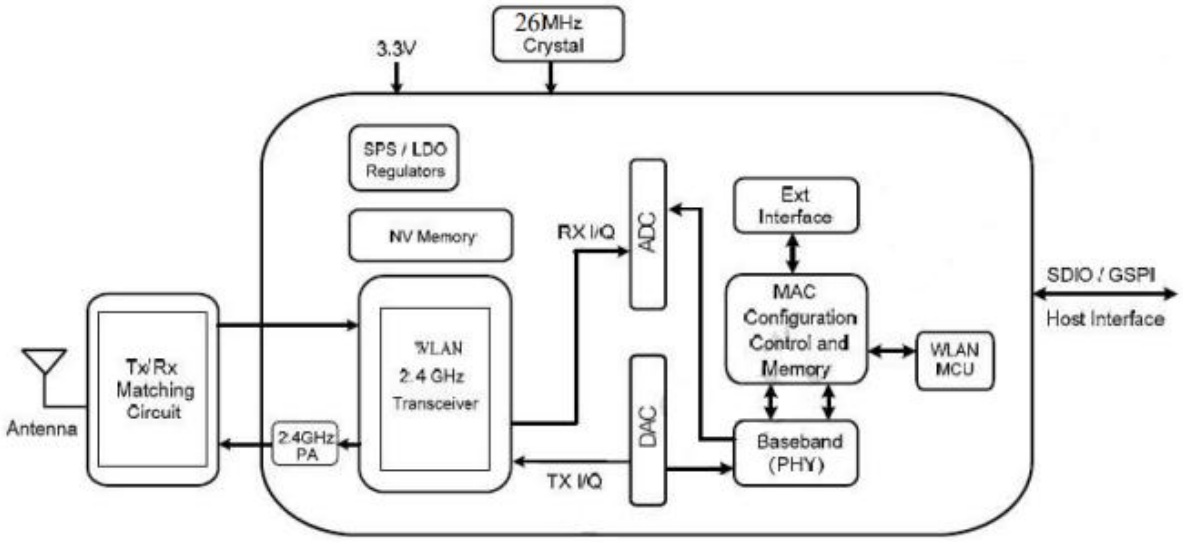
- Operate at ISM frequency bands (2.4GHz)
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n
- WiFi 1 T 1 R allow data rates supporting up to 72.2Mbps PHY rates

Host Interface

- SDIOV1.1/2.0 Interface for WiFi

3. Block Diagram

Single-Band 11n (1x1) Solution



4. General Specification

4.1 WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 16dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
	Note: 11n MCS7 HT40 and 11b 11M power is calibrated, other rate	
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 11Mbps PER @ -82 dBm	≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 54Mbps PER @ -71 dBm	≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ -65 dBm	≤-67

5. ID setting information

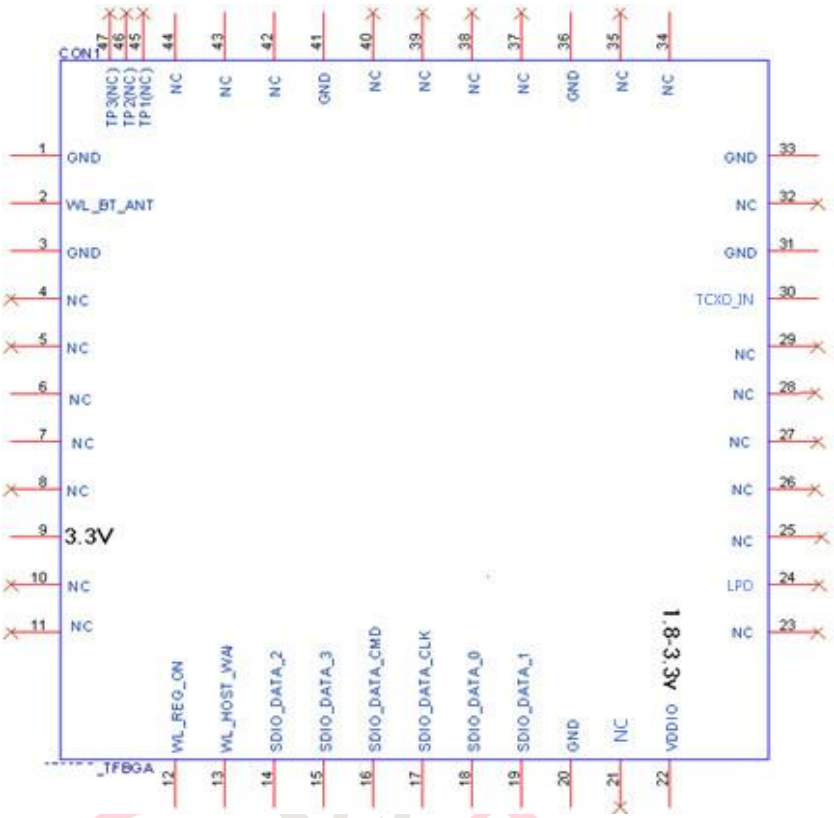
WI-FI

Vendor ID	TBD
Product ID	TBD

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	RF	I/O	RF OUTPUT	
3	GND		Ground connections	
4~8	NC		Floating (NC)	
9	3.3V	P	main power input	3.3V
10	NC		Floating (NC)	
11	NC		Floating (NC)	
12	WL_REG_ON		WL_REG_ON, external pull low shutdown RTL8189FTV	3.3V
13	WL_HOST_WAKE	O	WLAN WAKE HOST	VDIO
14	SDIO_DATA_2	I/O	SDIO_D2	VDIO
15	SDIO_DATA_3	I/O	SDIO_D3	VDIO
16	SDIO_DATA_CMD	I/O	SDIO_CMD	VDIO
17	SDIO_DATA_CLK	I	SDIO_CLK	VDIO
18	SDIO_DATA_D0	I/O	SDIO_D0	VDIO
19	SDIO_DATA_D1	I/O	SDIO_D1	VDIO
20	GND		Ground connections	
21	NC		Floating (NC)	
22	VDIO	P	1.8~3.3V	
23	NC		Floating (NC)	
24	LPO		CLK_REQ,if not used please NC.	
25~29	NC		Floating (NC)	
30	TCXO_IN		26MHz_IN,if not used please NC.	
31	GND		Ground connections	
32	NC		Floating (NC)	
33	GND		Ground connections	
34~35	NC		Floating (NC)	
36	GND		Ground connections	
37~40	NC		Floating (NC)	
41	GND		Ground connections	
42~44	NC		Floating (NC)	

P:POWER I:INPUT O:OUTPUT

7. Electrical Specifications

7.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
VCC33	3.0	3.3	3.6	V
VDDIO	1.62	1.8 or 3.3	3.6	V

7.2 Power Consumption

Mode	Status	Power(mA)	Note
OS Windows XP	Link	130	
	RX	130	20M
	TX	190	20M(MCS7)

7.3 SDIO interface Timing Diagram

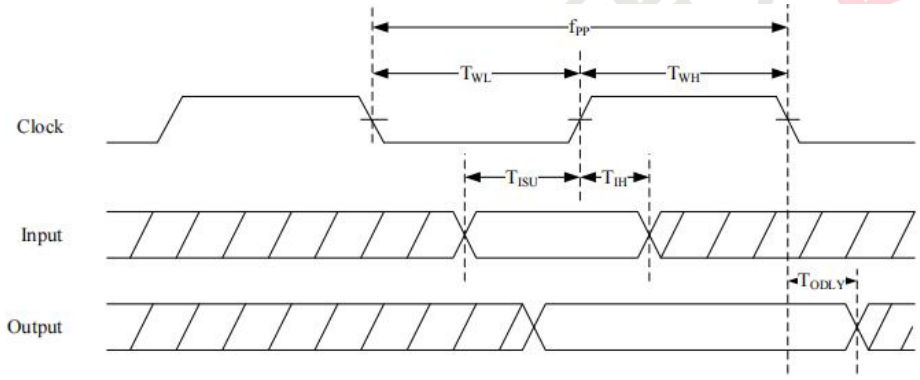


Figure 3. SDIO Interface Timing

Table 10 SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns

		HS	7		
T_{ISU}	Input setup time	DEF	5		ns
		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

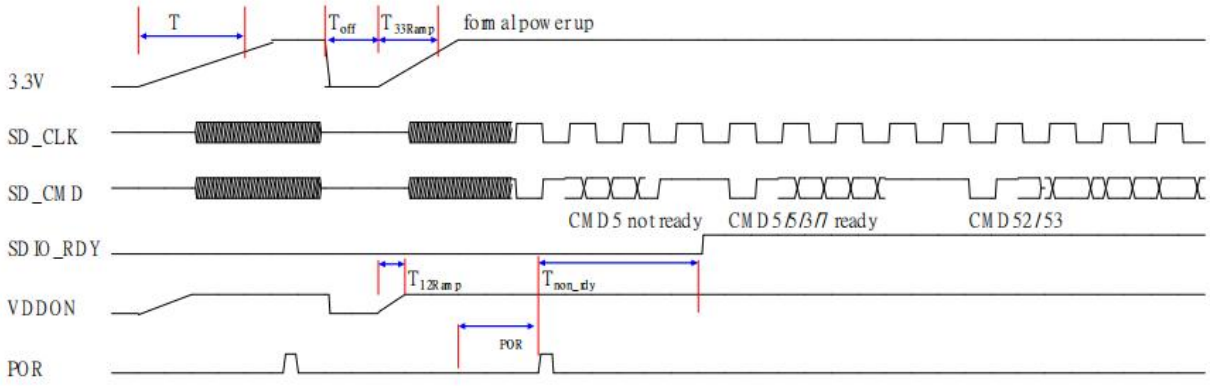
■ SDIO Interface Signal Level

The SDIO signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8189FTV-VQ1 SDIO interface via VDIO_SDIO pin (pin19).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.2.2.

7.3.1 SDIO Power-on sequence

After power on, the SDIO interface is selected by RTL8189FTV-VQ1 automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended:



Variable definition:

T33ramp': The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

Toff : The duration the 3.3V is cut off before formal power up.

T33ramp: The 3.3V main power ramp up duration

T12ramp: The internal 1.2V ramp up duration.

T_{POR}: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T_{non_rdy}: SDIO not ready duration, in this state, RTL8723AS may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuits during T_{non_rdy} duration. After autoload done, the SDIO responds command with ready bit set. After CMD5/ 5/ 3/ 7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

The typical timing spec is shown as follows:

Table 11 SDIO Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	0.2	0.5	2.5	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

7.3.2 Power off by chip_en sequence

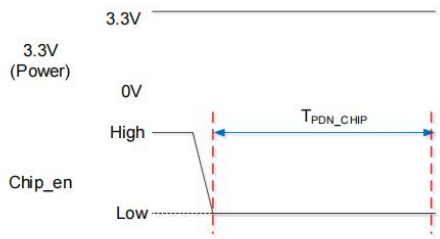


Figure 4. Power Off by chip_en Sequence

Table 12. Power Off by WL# and BT_DIS# Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PDN_CHIP}	10	100	--	ms	Chip_en keep low duration

Chip_en can externally shutdown the RTL8189FTV –VQ1 when chip_en is pulled low. The keeping low duration must be more than T_{PDN_CHIP}

7.3.3 Power off by 3.3V power sequence

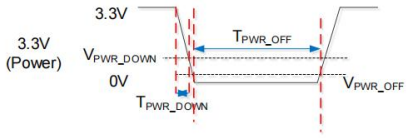


Figure 5. Power Off by 3.3V power Sequence

Table 13. Power Off by 3.3V power Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PWR_OFF}	10	100	--	ms	3.3V power off time
V_{PWR_OFF}	--	--	0.4	V	3.3V power off voltage
V_{PWR_DOWN}	--	--	0.7	V	3.3V power down voltage
T_{PWR_DOWN}	--	--	10	ms	3.3V power down time

When 3.3V power off and on afterward, the voltage of 3.3V power must keep lower than V_{PWR_OFF}, and the 3.3V power keeping off duration must be more than T_{PWR_OFF}

7.3.4 SDIO Interface

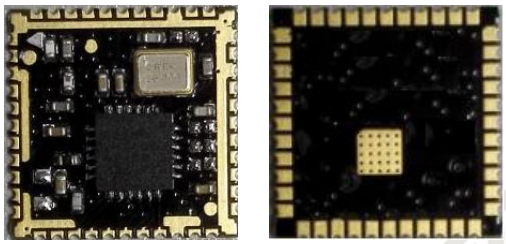
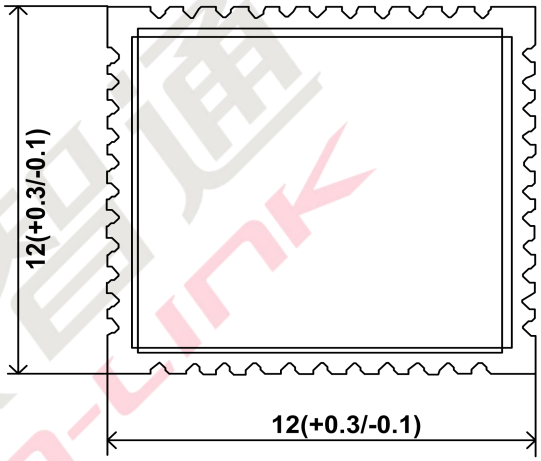
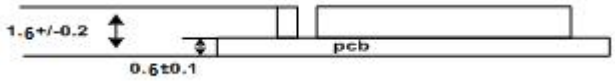
Symbol	Type	Pin	Description
SD_CLK	I	17	SDIO Clock Input
SD_CMD	I/O	16	SDIO Command Input
SD_D0	I/O	18	SDIO Data Line 0
SD_D1	I/O	19	SDIO Data Line 1
SD_D2	I/O	14	SDIO Data Line 2
SD_D3	I/O	15	SDIO Data Line 3

7.3.5 GPIO Interface

Symbol	Type	Pin	Description
GSPI_CLK	I	17	GSPI Clock Input
GSPI_MOSI	I	16	GSPI Data Input
GSPI_MISO	O	18	GSPI Data Out
GSPI_SIRQ	O	19	GSPI Interrupt
GSPI_SCSn	I	15	GSPI Chip Select Bar

8. Size reference

8.1 Module Picture

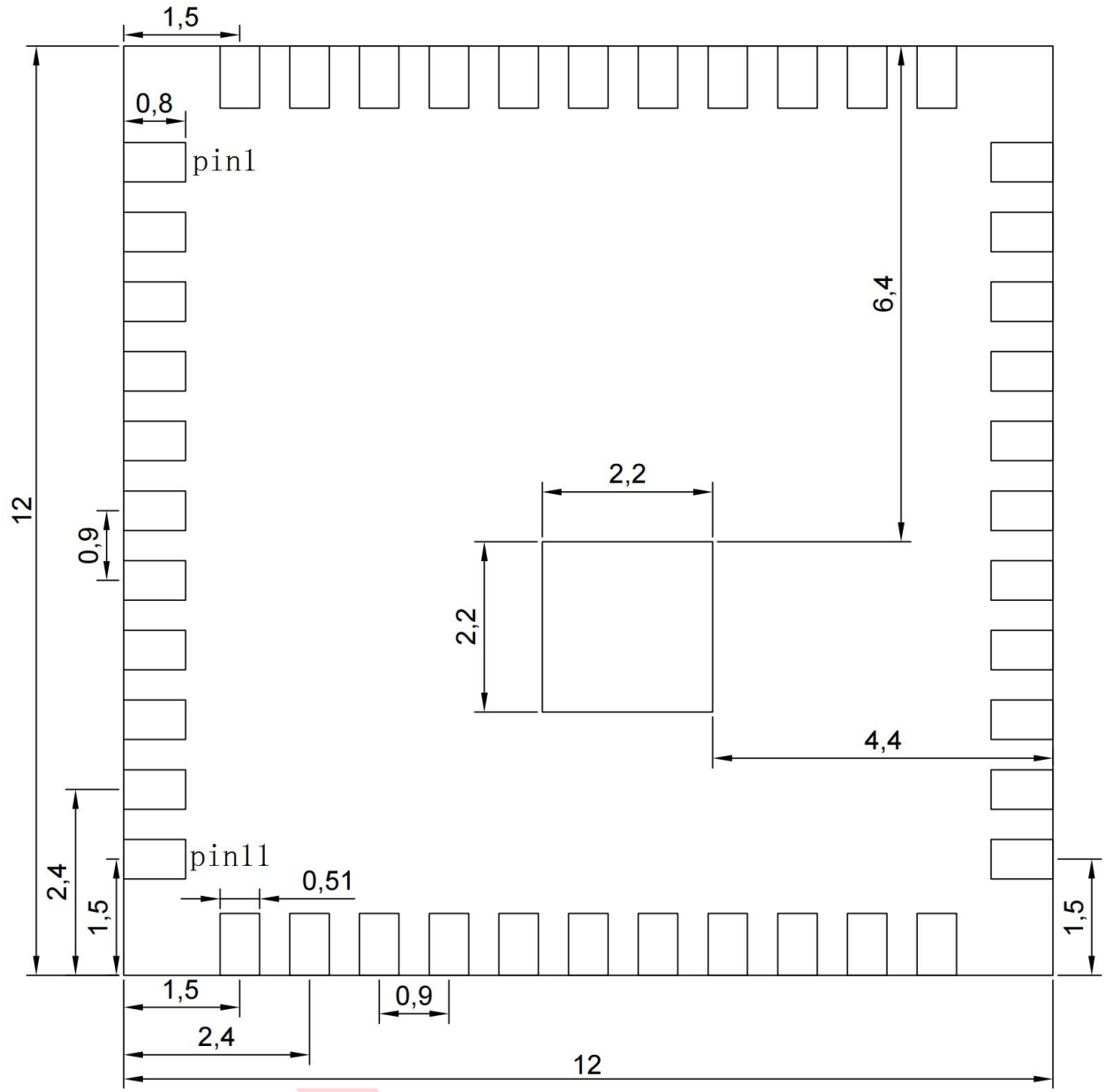
<table>
<tr><td>L x W : 12 x 12 (+0.3/-0.1) mm
  </td><td> 
</td></tr>
<tr><td>H: 1.6 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>0.48g</td></tr>
</table>

8.2 List of certified information

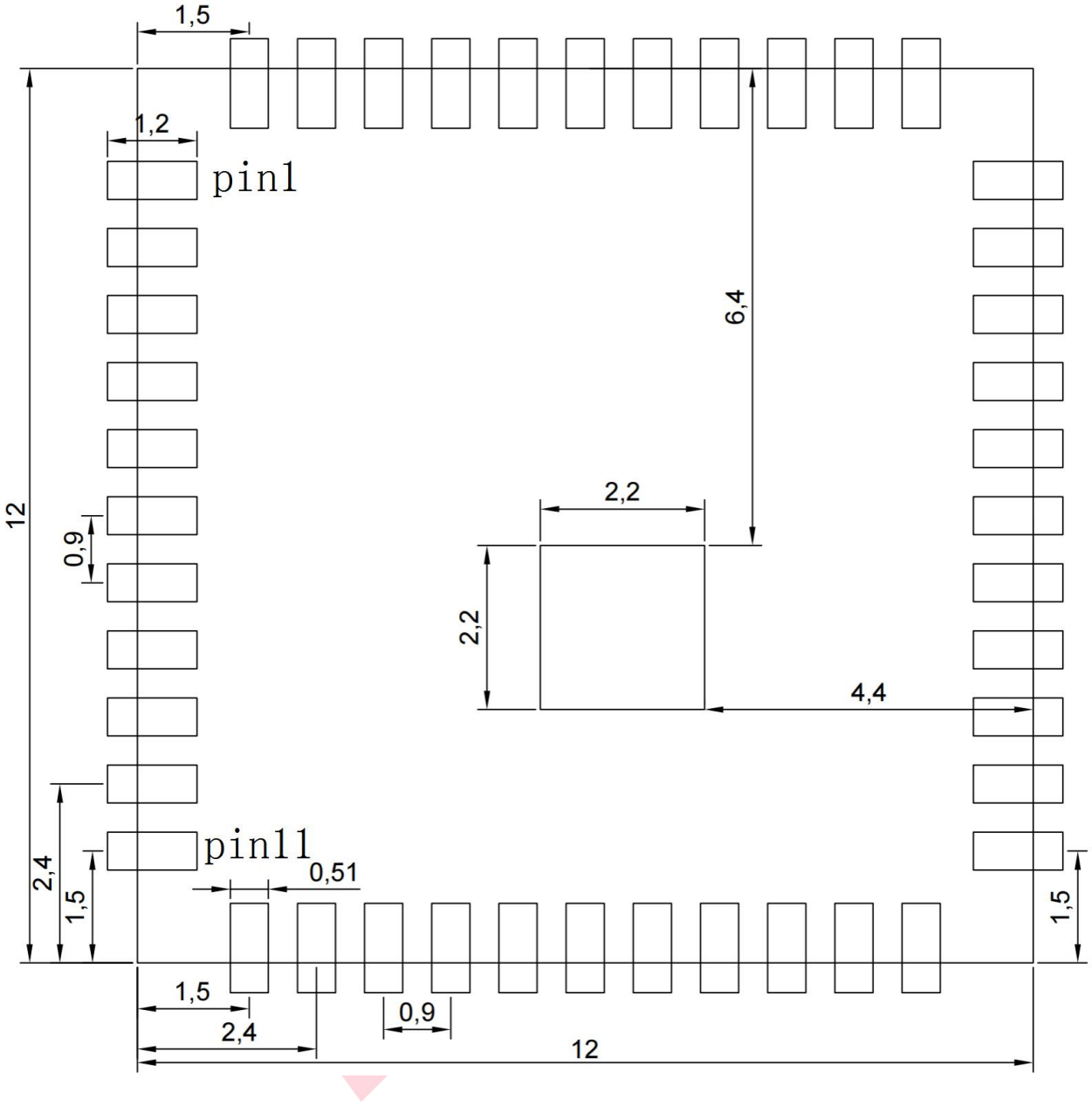
Certification project	Certificate number
SRRC	CMIIT ID:2023DP13675(M)
FCC	2AATL-F89FTSM13
CE	TBD
IC	TBD
NCC	TBD
KCC	TBD
TELEC	TBD
Brazil	TBD
Argentina	TBD
Japan	TBD

8.4 Physical Dimensions

<TOP View>


1,5
0,8
pin1
6,4
2,2
12
0,9
2,2
4,4
pin11
2,4
1,5
0,51
1,5
1,5
0,9
2,4
12

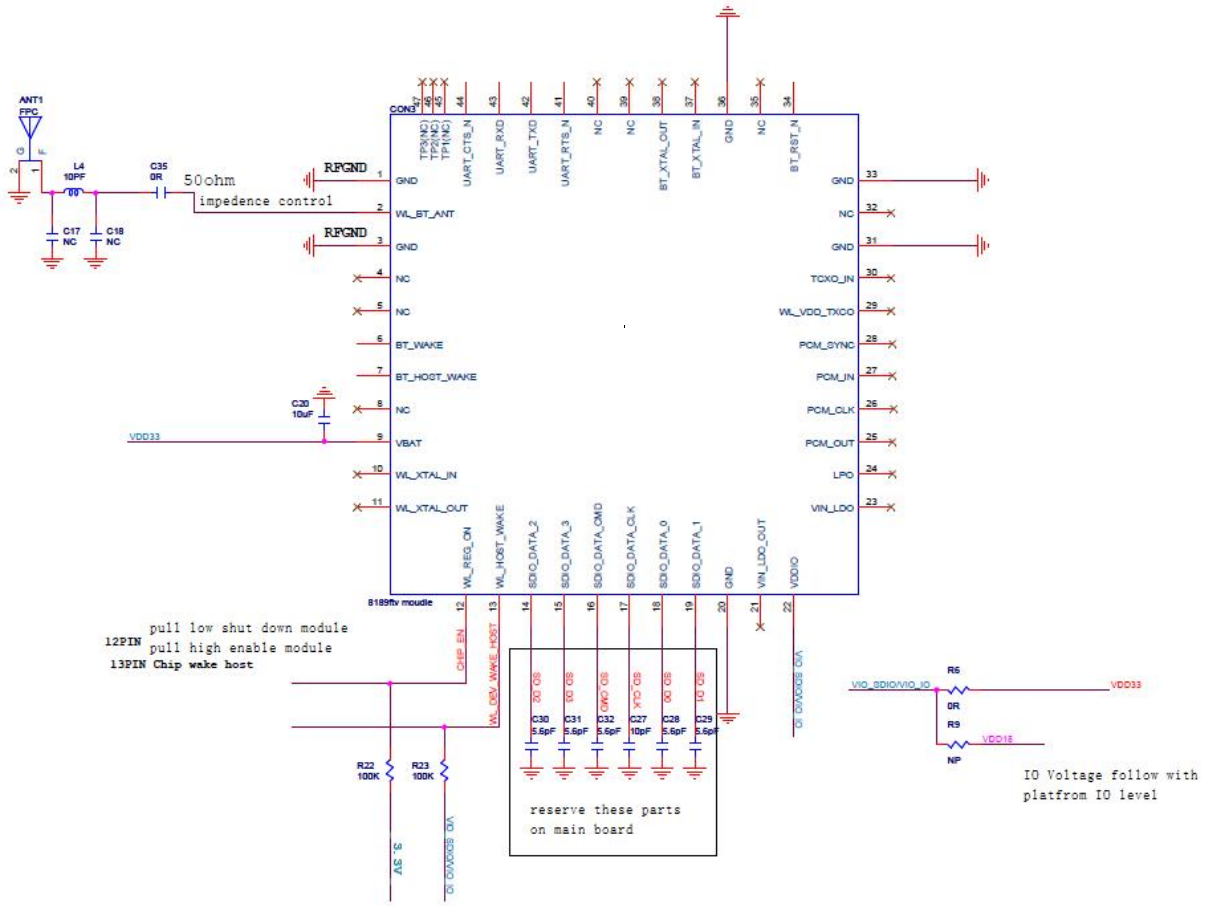
8.5 Layout Recommendation



9. The Key Material List

Item	Part Name	Description	Manufacturer
1	TVS	0402 4V 0.05pF 15KV TVS	Murata,Sunlord，JieJie Semiconductor
2	Crystal	26Mhz 3225 ±10ppm,10.5pF	ECEC,HOSONIC,TKD,JWT
3	Chipset	RTL8189FTV-VQ1-CG	Realtek
4	PCB	F89FTSM13,black,4L,FR4,Tg150,Au,12 X12X0.6mm	XY-PCB,KX-PCB,Sunlord,SL-PCB

10. Reference Design



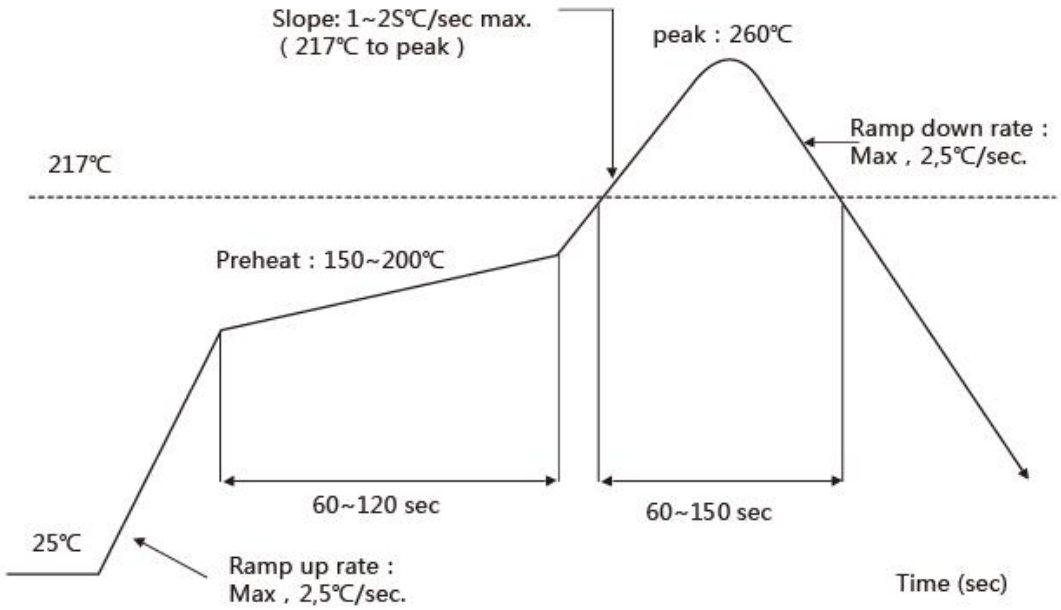
11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Reflow 260° C and holding time at least 10seconds

Number of Times : ≤2 times



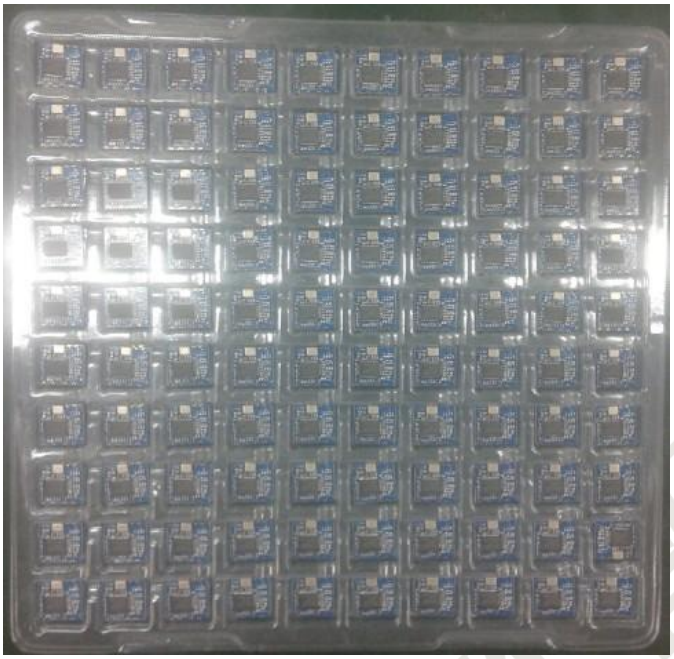
WIFI module installed note:

1. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil
2. Take and use the WIFI module, please insure the electrostatic protective measures.
3. Reflow soldering temperature should be according to the customer the main size of the products, such as the temperature set at 250 + 5 ℃ for the MID motherboard.

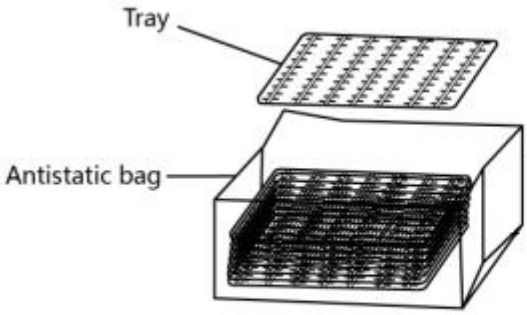
12. Package

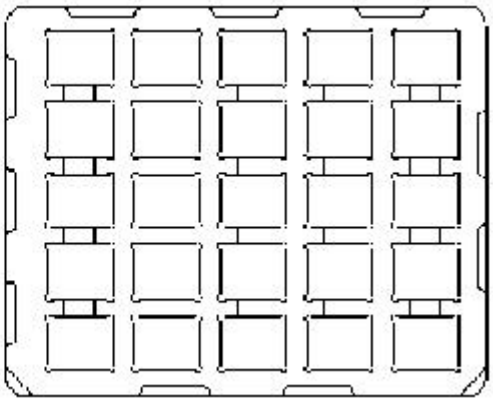
12.1 Blister packaging

A piece of 100pcs



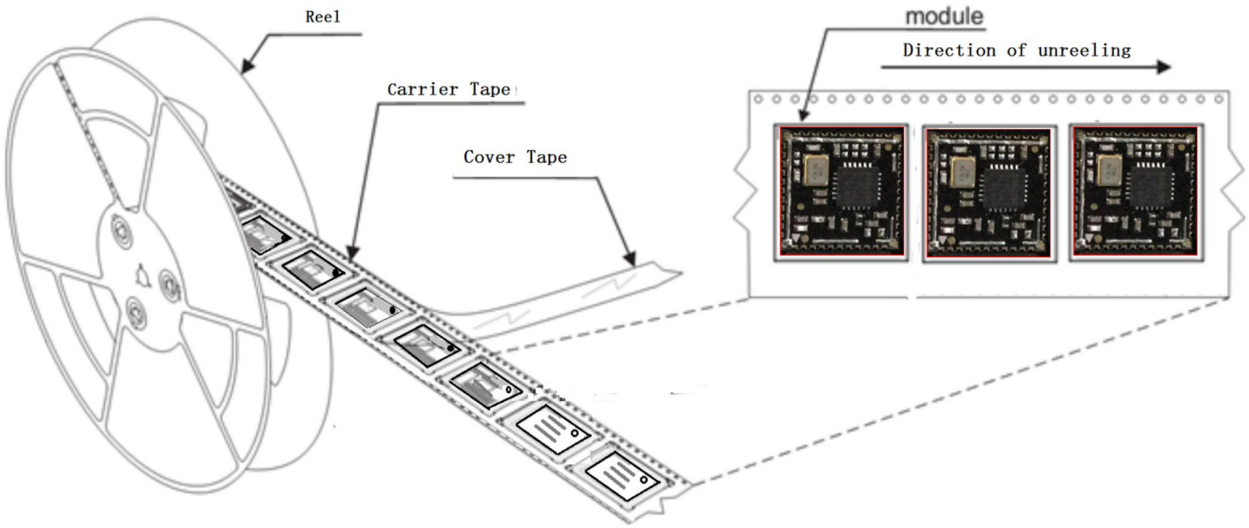
Use pallet packaging for less than 300 pieces



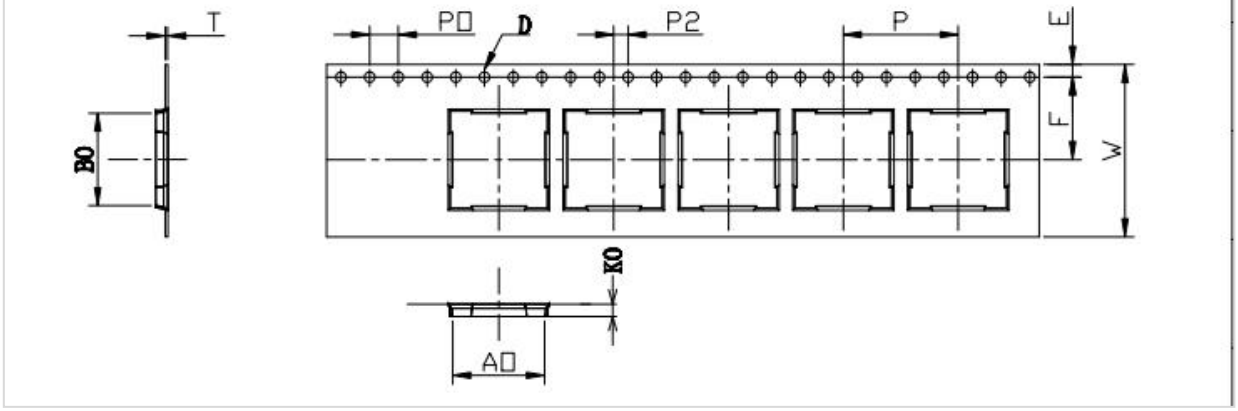


12.2 Reel

A roll of 1500pcs

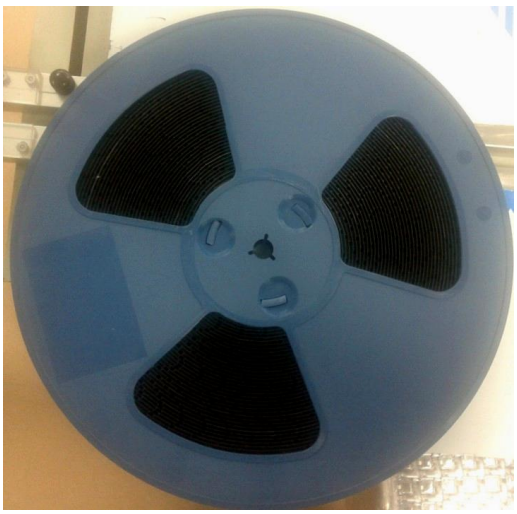


ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



12.3 Packaging Detail

the take-up package



Using self-adhesive tape
Color of plastic disc: blue

NY bag size:460mm*385mm

size ： 350*350*35mm

The packing case size:350*210*370mm

13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more